REMARKS

Claims 1-14 are pending in this patent application. Claims 1-14 are rejected by the Examiner.

The Examiner stated that the oath or declaration is missing from the application papers.

Applicants have enclosed a signed declaration in compliance with 37 C.F.R. §1.67(a) identifying this application by application number and filing date.

The Examiner requested a revised abstract to correct some misspellings.

Applicants have amended the abstract to correct the misspellings. No new matter was added.

The Examiner indicted that the abstract was merely borrowed language of the claims and requested an amended abstract.

Applicants disagree. The abstract, as amended, enables the reader thereof, regardless of his or her degree of familiarity with patent documents, to ascertain quickly the character of the subject matter covered by the technical disclosure, as required by 37 C.F.R. §1.72 and MPEP 608.01(b). Applicants' claimed invention is a method of operating a processor including concatenating a first and second word to produce an intermediate result, shifting the intermediate result by a specified shift amount and storing the shifted intermediate result in a third word. Accordingly, applicants' abstract is proper under 37 C.F.R. §1.72 and the Examiner's requirement should be withdrawn.

The Examiner rejected claims 1 and 8 under 35 U.S.C. 102(b) as being clearly anticipated by any one of U.S. Patent 5,717,760 (Satterfield), U.S. Patent 5,652,583 (Kang), U.S. Patent 5,600,812 (Park), U.S. Patent 5,436,626 (Fujiwara et al.) or U.S. Patent 5,363,448 (Koopman, Jr. et al.).

Applicants' claim 1 calls for "...concatenating a first word and a second word to produce an intermediate result, shifting the intermediate result by a specified shift amount, and storing the shifted intermediate result in a third word."

Satterfield neither describes nor suggests concatenating a first word and a second word to produce an intermediate result, as claimed in claim 1. On the contrary, Satterfield discloses two

arrays of different widths and two arrays of the same width, each producing an intermediate result having a width of one of the two arrays. (see col. 21, line 37-67, col. 22, lines 1-53). Thus, Satterfield discloses either width truncation or no width truncation in the intermediate result, rather than concatenation.

As is known to one skilled in this art, concatenation is taking two or more separately located things and placing them side-by-side next to each other so that they can now be treated as one thing. In computer programming and data processing, two or more character strings are sometimes concatenated for the purpose of saving space or so that they can be addressed as a single item. New words can be made by concatenating two existing words. For example, "airline" is a concatenation of the words "air" and "line" into a new word. As defined in Random House Webster's Dictionary 3rd edition (©1998), page 144, concatenate means to link together, as in a chain. Accordingly, claim 1 is not anticipated by Satterfield.

Applicants' claim 8 calls for "...concatenate a first word and a second word to produce an intermediate result..." For at least the reasons stated with respect to claim 1, claim 8 is not anticipated by Satterfield.

Kang neither describes nor suggests shifting the intermediate result by a specified shift amount, and storing the shifted intermediate result in a third word, as claimed in claim 1. On the contrary, Kang, at col. 3, lines 12-17, discloses "(t)he VLC encoding and segmenting apparatus produces variable length codes (VLCs), represented by variable-length code words and their lengths, concatenates them together and segments the concatenated bit string into n-bit words for the transmission thereof." Thus, Kang concatenates and segments into multiple n-bit words and not a single intermediate result. Accordingly, claim 1 ("storing the shifted intermediate result in a third word") and claim 8 ("store the shifted intermediate result in a third word") are not anticipated by Kang.

Park neither describes nor suggests concatenating a first word and a second word to produce an intermediate result. Instead, Park discloses decoding a variable length code (first word) wherein the decoded result and a bit length are stored in a single location (second word). The bit length is then used to shift and store the decoded result in the second word. More specifically, Park discloses "...VLC decoder includes a look-up table memory that stores, in a storage location with the same address as the storage location of the decoding result for a

variable-length code, an indication of the bit-length of that variable-length code. When one of the variable-length codes is decoded, both the decoding result and the indication of the bit-length of the variable-length code that has been decoded are read from the look-up table memory. The bit-length indication is used to shift the variable-length code within the input address register so as to place the next variable-length-code (VLC) word directly into the final position within the address register." (col. 3, lines 30-43). Accordingly, claim 1 ("concatenating a first word and a second word to produce an intermediate result") and claim 8 ("concatenate a first word and a second word to produce an intermediate result") are not rendered obvious by Park.

Fujiwara et al. neither describes nor suggests concatenating a first word and a second word to produce an intermediate result and shifting the intermediate result by a specified shift amount. In direct contrast, Fujiwara et al. describes shifting and concatenating. More specifically, Fujiware et al. discloses "(a)n OR circuit (38) combines the shifted variable-length codeword with previous variable-length codeword bits to form a concatenated sequence which is stored in upper and lower latches (53, 54)." (see Abstract). Accordingly, claim 1 ("concatenating a first word and a second word to produce an intermediate result and shifting the intermediate result by a specified shift amount") and claim 8 ("concatenate a first word and a second word to produce an intermediate result and shift the intermediate result by a specified shift amount") are not rendered obvious by Fujiwara et al.

Koopman, Jr. et al. neither describes nor suggests shifting the intermediate result by a specified shift amount and storing the shifted intermediate result in a third word. Koopman Jr. et al. merely discloses a method of receiving a word (first word) to generate an encrypted word (second word). More specifically, Koopman, Jr. et al. discloses "...an encryption, such as a linear feedback shift register pseudorandom number generation operation, is performed on a word comprising a pair of concatenated, independently generated numbers, which may themselves be encrypted (such as pseudorandom numbers) and the result transmitted to a receiving module where a decryption, such as a reverse pseudorandom number generation operation, recovers the concatenated numbers for cryptographic authentication." (Col. 3, lines 3-11) Accordingly, claim 1 ("shifting the intermediate result by a specified shift amount and storing the shifted intermediate result in a third word") and claim 8 ("shift the intermediate result

by a specified shift amount and store the shifted intermediate result in a third word") are not rendered obvious by Koopman, Jr. et al.

The Examiner rejected claims 2-7 and 9-14 under 35 U.S.C. 103(a) as being unpatentable over any one of Satterfield, Kang, Park, Fujiwara et al. or Koopman, Jr. et al.

Claims 1 and 8 are patentable over Satterfield, Kang, Park, Fujiwara et al. and Koopman, Jr. et al., whether taken separately or in combination. Claims 2-7 depend upon, and further limit, claim 1. Claims 9-14 depend upon, and further limit, claim 8. Accordingly, claims 2-7 and 9-14 are patentable over Satterfield, Kang, Park, Fujiwara et al. and Koopman, Jr. et al., whether taken separately or in combination.